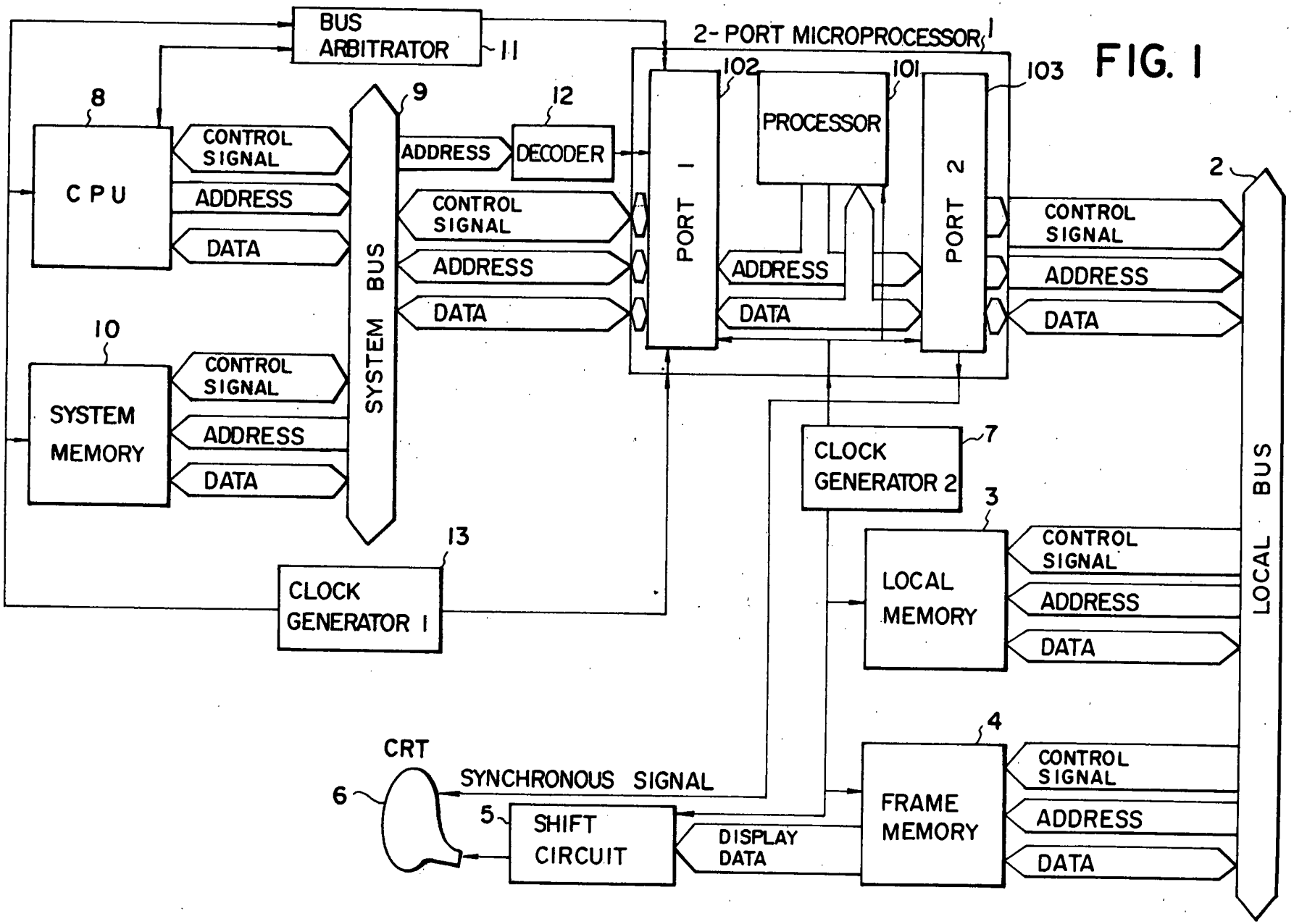

BUS ARBITRATOR
11
2-PORT MICROPROCESSOR
1
FIG. 1
8
CPU
CONTROL SIGNAL
ADDRESS
DATA
9
SYSTEM BUS
12
ADDRESS
DECODER
CONTROL SIGNAL
ADDRESS
DATA
102
PORT 1
PROCESSOR
101
PORT 2
103
ADDRESS
DATA
2
CONTROL SIGNAL
ADDRESS
DATA
LOCAL BUS
10
SYSTEM MEMORY
CONTROL SIGNAL
ADDRESS
DATA
CLOCK GENERATOR 2
7
3
LOCAL MEMORY
CONTROL SIGNAL
ADDRESS
DATA
13
CLOCK GENERATOR 1
CRT
6
SYNCHRONOUS SIGNAL
5
SHIFT CIRCUIT
DISPLAY DATA
4
FRAME MEMORY
CONTROL SIGNAL
ADDRESS
DATA

FIG. 2

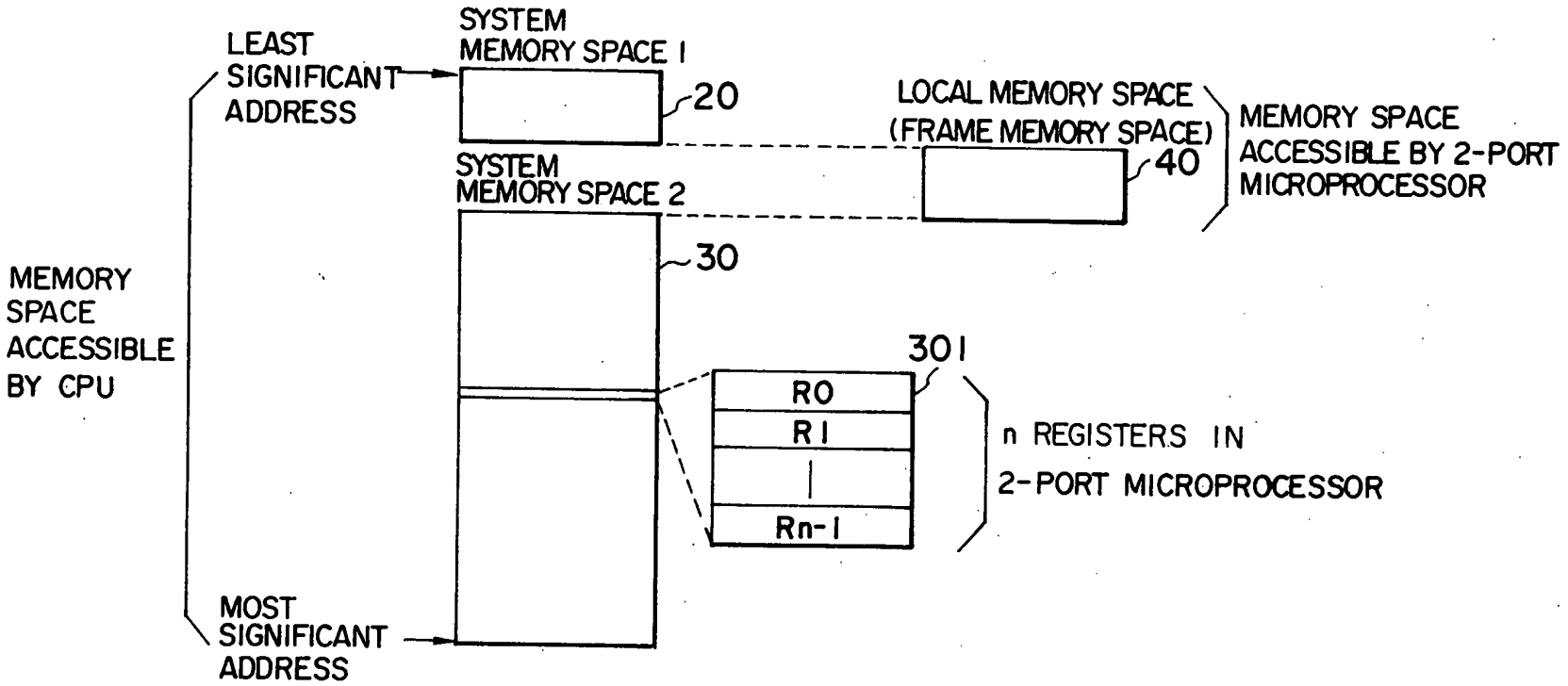

LEAST
SIGNIFICANT
ADDRESS
SYSTEM
MEMORY SPACE 1
20
LOCAL MEMORY SPACE
(FRAME MEMORY SPACE)
40
MEMORY SPACE
ACCESSIBLE BY 2-PORT
MICROPROCESSOR
SYSTEM
MEMORY SPACE 2
30
MEMORY
SPACE
ACCESSIBLE
BY CPU
301
R0
R1
Rn-1
n REGISTERS IN
2-PORT MICROPROCESSOR
MOST
SIGNIFICANT
ADDRESS

FIG. 3

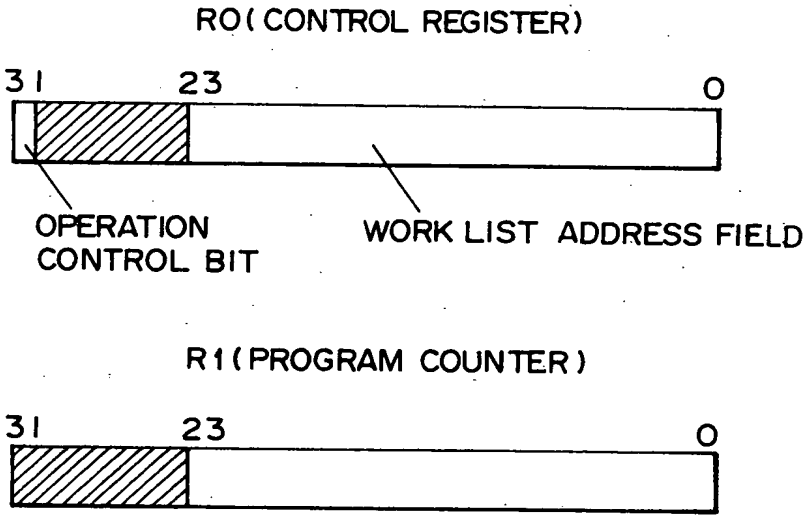

R0 (CONTROL REGISTER)
31
23
0
OPERATION
CONTROL BIT
WORK LIST ADDRESS FIELD
R1 (PROGRAM COUNTER)
31
23
0

FIG. 4

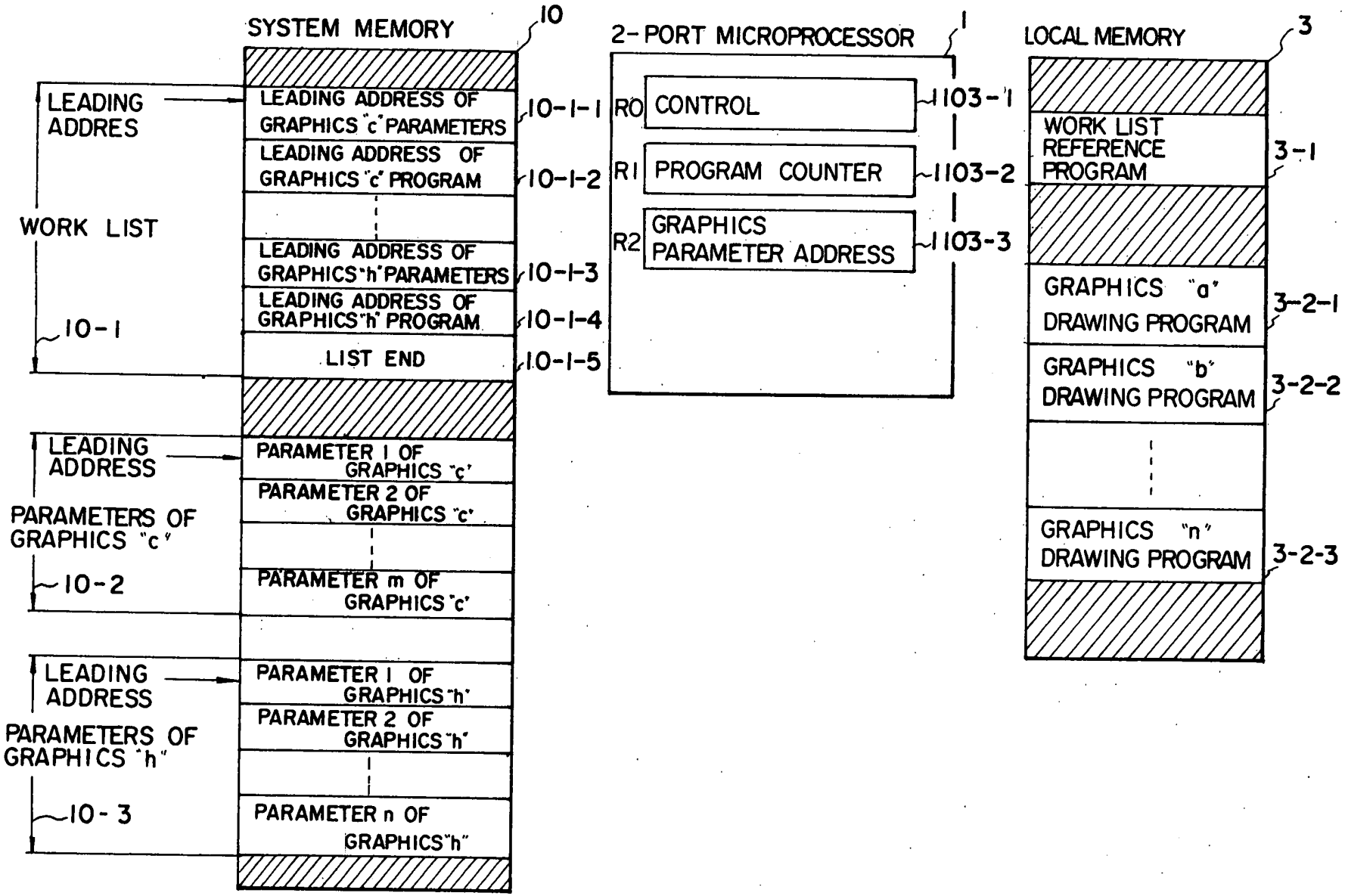
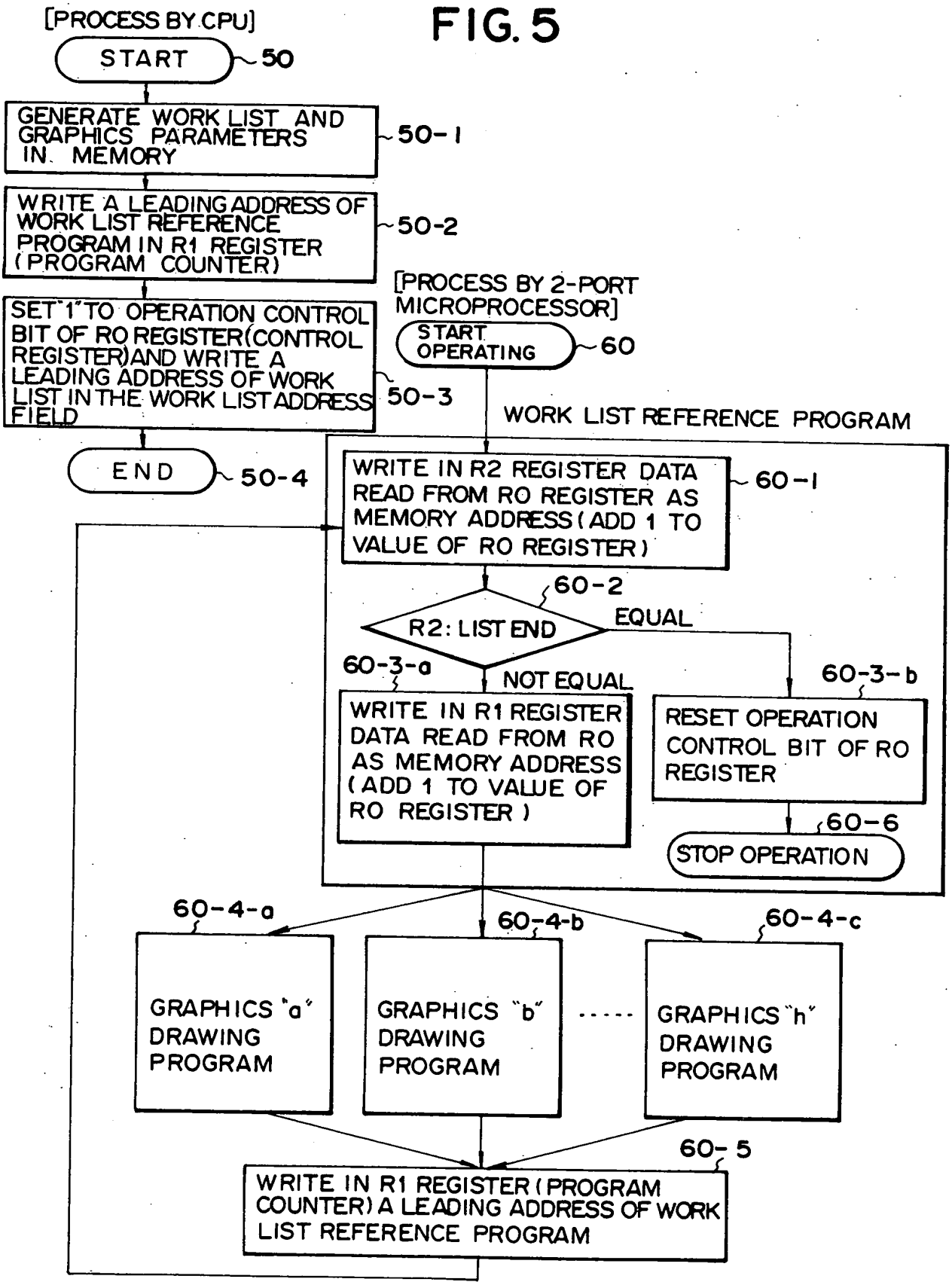

SYSTEM MEMORY
10
LEADING ADDRES
LEADING ADDRESS OF GRAPHICS "c" PARAMETERS
10-1-1
LEADING ADDRESS OF GRAPHICS "c" PROGRAM
10-1-2
WORK LIST
LEADING ADDRESS OF GRAPHICS "h" PARAMETERS
10-1-3
LEADING ADDRESS OF GRAPHICS "h" PROGRAM
10-1-4
10-1
LIST END
10-1-5
LEADING ADDRESS
PARAMETER 1 OF GRAPHICS "c"
PARAMETER 2 OF GRAPHICS "c"
PARAMETERS OF GRAPHICS "c"
PARAMETER m OF GRAPHICS "c"
10-2
LEADING ADDRESS
PARAMETER 1 OF GRAPHICS "h"
PARAMETER 2 OF GRAPHICS "h"
PARAMETERS OF GRAPHICS "h"
PARAMETER n OF GRAPHICS "h"
10-3
2-PORT MICROPROCESSOR
1
R0
CONTROL
1103-1
R1
PROGRAM COUNTER
1103-2
R2
GRAPHICS PARAMETER ADDRESS
1103-3
LOCAL MEMORY
3
WORK LIST REFERENCE PROGRAM
3-1
GRAPHICS "a" DRAWING PROGRAM
3-2-1
GRAPHICS "b" DRAWING PROGRAM
3-2-2
GRAPHICS "n" DRAWING PROGRAM
3-2-3

FIG. 5


[PROCESS BY CPU]
START
50
GENERATE WORK LIST AND GRAPHICS PARAMETERS IN MEMORY
50-1
WRITE A LEADING ADDRESS OF WORK LIST REFERENCE PROGRAM IN R1 REGISTER (PROGRAM COUNTER)
50-2
SET "1" TO OPERATION CONTROL BIT OF RO REGISTER (CONTROL REGISTER) AND WRITE A LEADING ADDRESS OF WORK LIST IN THE WORK LIST ADDRESS FIELD
50-3
END
50-4
[PROCESS BY 2-PORT MICROPROCESSOR]
START OPERATING
60
WORK LIST REFERENCE PROGRAM
WRITE IN R2 REGISTER DATA READ FROM RO REGISTER AS MEMORY ADDRESS (ADD 1 TO VALUE OF RO REGISTER)
60-1
60-2
R2: LIST END
EQUAL
NOT EQUAL
60-3-a
60-3-b
WRITE IN R1 REGISTER DATA READ FROM RO AS MEMORY ADDRESS (ADD 1 TO VALUE OF RO REGISTER)
RESET OPERATION CONTROL BIT OF RO REGISTER
60-6
STOP OPERATION
60-4-a
60-4-b
60-4-c
GRAPHICS "a" DRAWING PROGRAM
GRAPHICS "b" DRAWING PROGRAM
GRAPHICS "h" DRAWING PROGRAM
60-5
WRITE IN R1 REGISTER (PROGRAM COUNTER) A LEADING ADDRESS OF WORK LIST REFERENCE PROGRAM

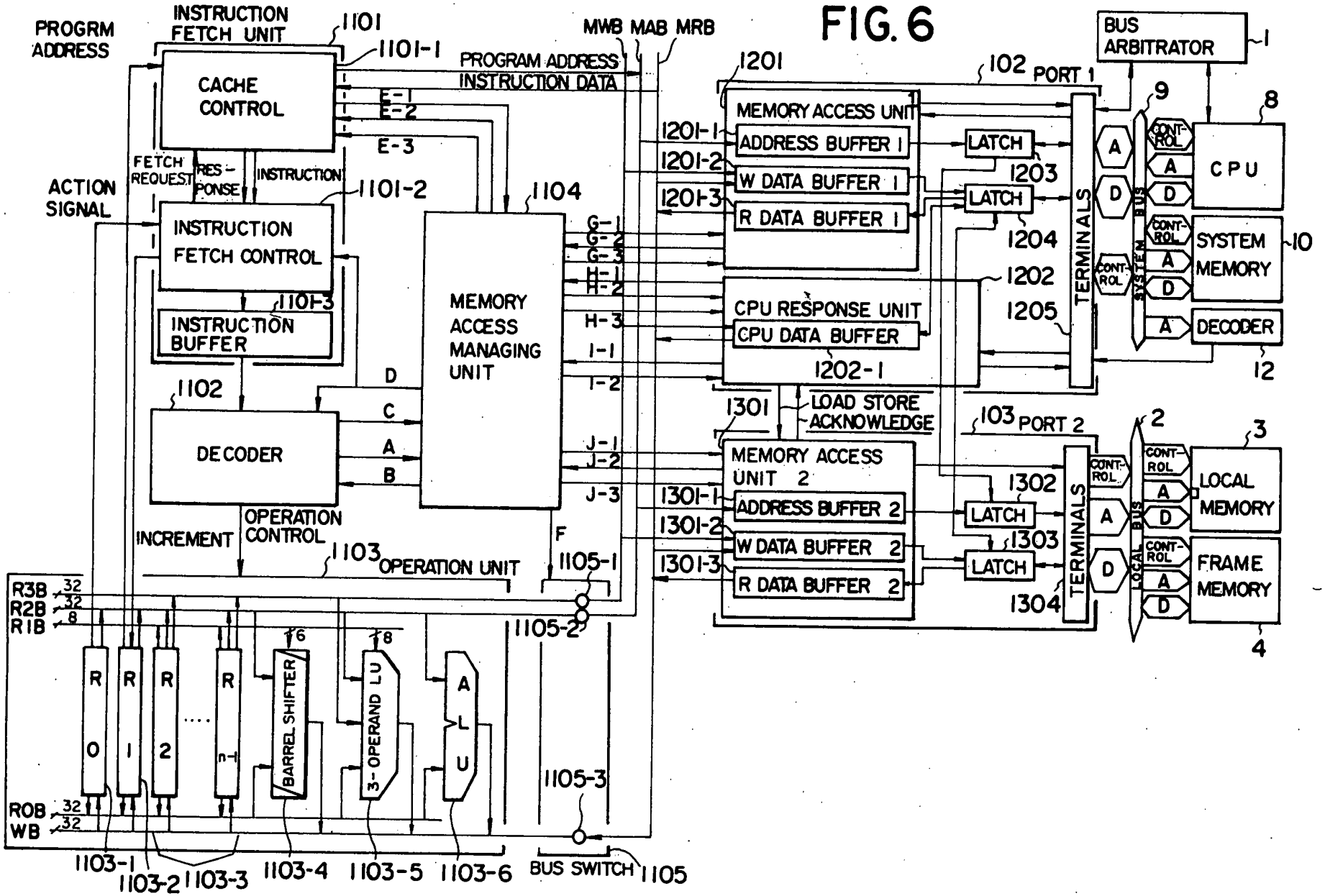

PROGRM ADDRESS
INSTRUCTION FETCH UNIT
1101
1101-1
CACHE CONTROL
PROGRAM ADDRESS
INSTRUCTION DATA
E-1
E-2
E-3
FETCH REQUEST
RES-PONSE
INSTRUCTION
ACTION SIGNAL
1101-2
INSTRUCTION FETCH CONTROL
1101-3
INSTRUCTION BUFFER
1104
MEMORY ACCESS MANAGING UNIT
G-1
G-2
G-3
H-1
H-2
H-3
I-1
I-2
J-1
J-2
J-3
D
C
A
B
F
1102
DECODER
INCREMENT
OPERATION CONTROL
1103
OPERATION UNIT
1105-1
1105-2
MWB MAB MRB
R3B 32
R2B 32
R1B 8
R0B 32
WB 32
R 0
R 1
R 2
R n-1
BARREL SHIFTER 6
3-OPERAND LU 8
ALU
1105-3
1103-1
1103-2
1103-3
1103-4
1103-5
1103-6
BUS SWITCH
1105
1201
MEMORY ACCESS UNIT
1201-1
ADDRESS BUFFER 1
1201-2
W DATA BUFFER 1
1201-3
R DATA BUFFER 1
1202
CPU RESPONSE UNIT
CPU DATA BUFFER
1202-1
1301
LOAD STORE ACKNOWLEDGE
MEMORY ACCESS UNIT 2
1301-1
ADDRESS BUFFER 2
1301-2
W DATA BUFFER 2
1301-3
R DATA BUFFER 2
102 PORT 1
LATCH
1203
LATCH
1204
1205
TERMINALS
103 PORT 2
1302
LATCH
1303
LATCH
1304
TERMINALS
BUS ARBITRATOR
1
9
8
CONT-ROL
A
D
CPU
SYSTEM BUS
SYSTEM MEMORY
10
DECODER
12
2
3
LOCAL BUS
LOCAL MEMORY
FRAME MEMORY
4

FIG. 6

FIG. 7

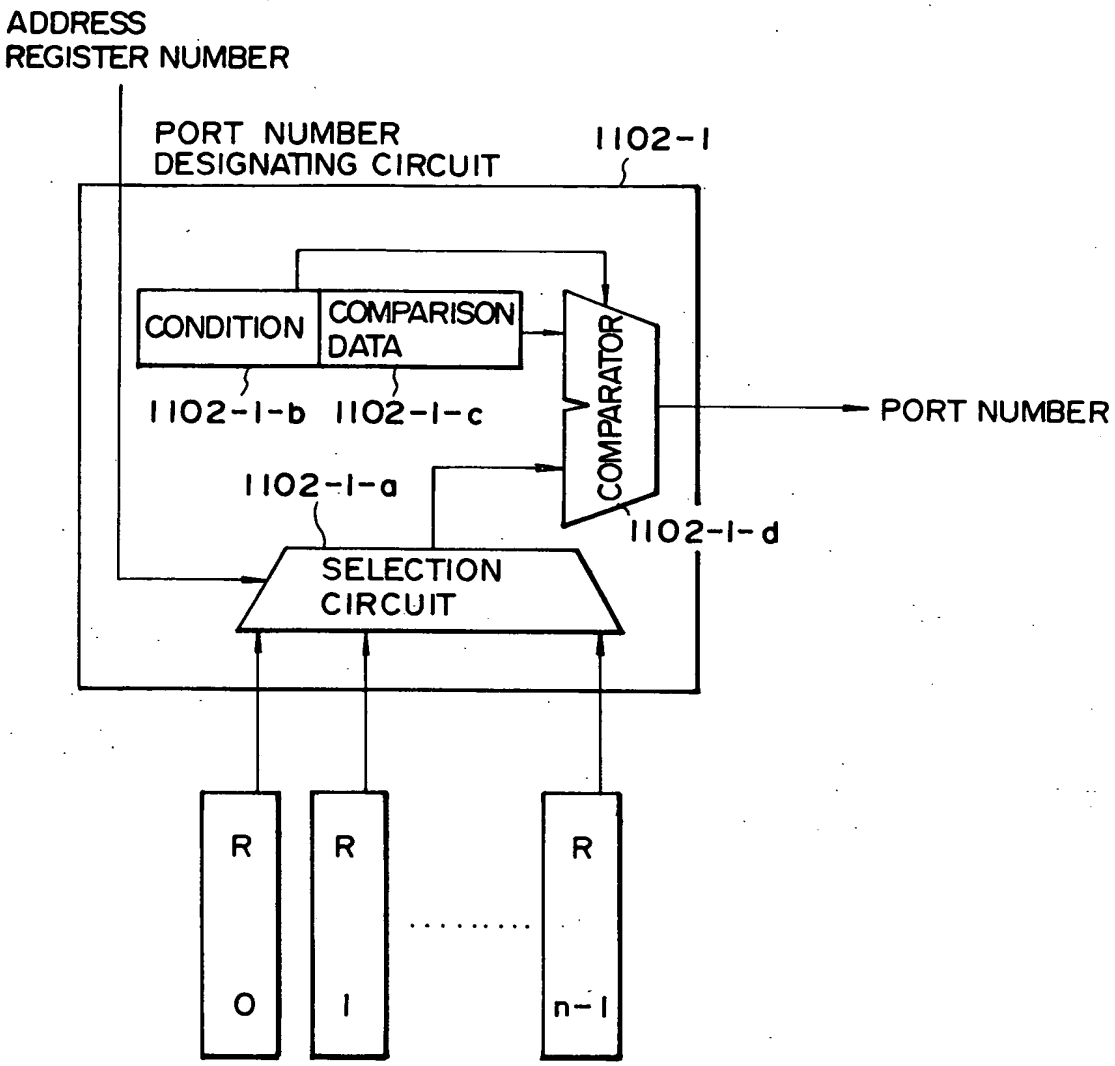


FIG. 8

PORT DESIGNATING METHOD	CONDITION BIT
IF DATA OF ADDRESS REGISTER ≧ COMPARISON DATA, DESIGNATE PORT 1	0
IF DATA OF ADDRESS REGISTER ≧ COMPARISON DATA, DESIGNATE PORT 2	1

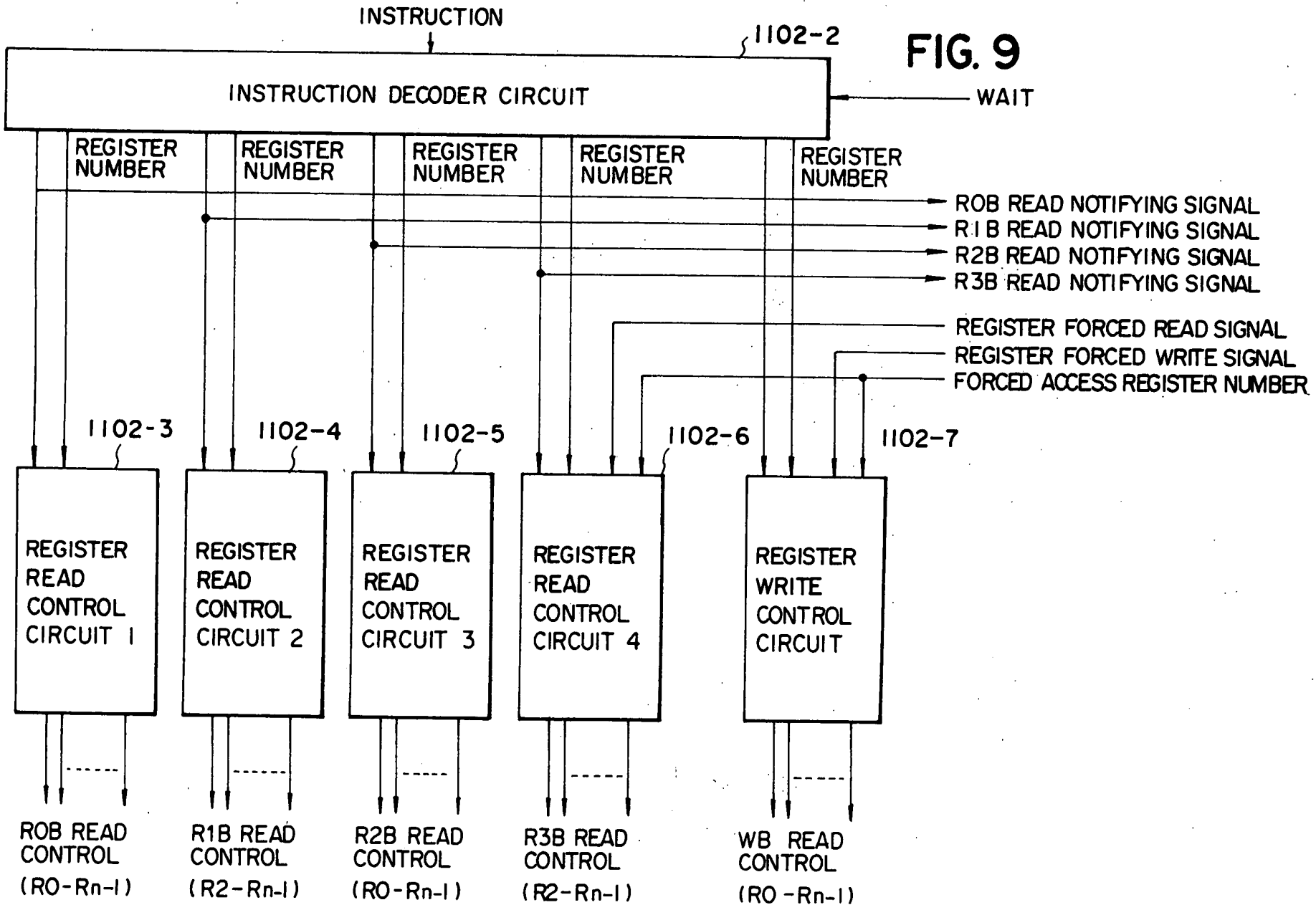

INSTRUCTION
1102-2
INSTRUCTION DECODER CIRCUIT
WAIT
REGISTER NUMBER
REGISTER NUMBER
REGISTER NUMBER
REGISTER NUMBER
REGISTER NUMBER
ROB READ NOTIFYING SIGNAL
R1B READ NOTIFYING SIGNAL
R2B READ NOTIFYING SIGNAL
R3B READ NOTIFYING SIGNAL
REGISTER FORCED READ SIGNAL
REGISTER FORCED WRITE SIGNAL
FORCED ACCESS REGISTER NUMBER
1102-3
1102-4
1102-5
1102-6
1102-7
REGISTER READ CONTROL CIRCUIT 1
REGISTER READ CONTROL CIRCUIT 2
REGISTER READ CONTROL CIRCUIT 3
REGISTER READ CONTROL CIRCUIT 4
REGISTER WRITE CONTROL CIRCUIT
ROB READ CONTROL (RO-Rn-1)
R1B READ CONTROL (R2-Rn-1)
R2B READ CONTROL (RO-Rn-1)
R3B READ CONTROL (R2-Rn-1)
WB READ CONTROL (RO-Rn-1)

FIG. 9

FIG. 10

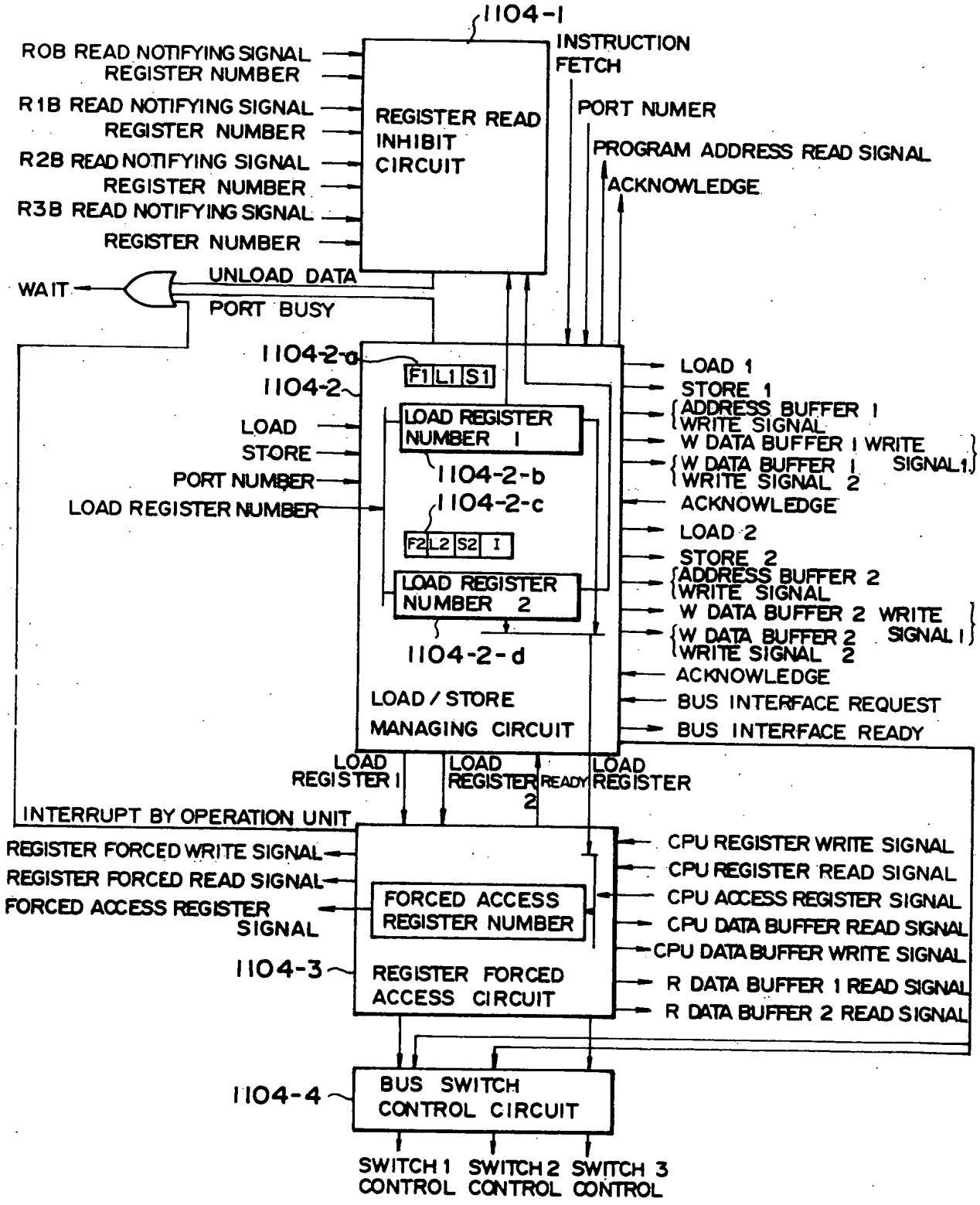

1104-1
ROB READ NOTIFYING SIGNAL
REGISTER NUMBER
R1B READ NOTIFYING SIGNAL
REGISTER NUMBER
R2B READ NOTIFYING SIGNAL
REGISTER NUMBER
R3B READ NOTIFYING SIGNAL
REGISTER NUMBER
REGISTER READ INHIBIT CIRCUIT
INSTRUCTION FETCH
PORT NUMER
PROGRAM ADDRESS READ SIGNAL
ACKNOWLEDGE
WAIT
UNLOAD DATA
PORT BUSY
1104-2-a
F1 L1 S1
1104-2
LOAD
STORE
PORT NUMBER
LOAD REGISTER NUMBER
LOAD REGISTER NUMBER 1
1104-2-b
1104-2-c
F2 L2 S2 I
LOAD REGISTER NUMBER 2
1104-2-d
LOAD / STORE MANAGING CIRCUIT
LOAD 1
STORE 1
ADDRESS BUFFER 1 WRITE SIGNAL
W DATA BUFFER 1 WRITE SIGNAL 1
W DATA BUFFER 1 WRITE SIGNAL 2
ACKNOWLEDGE
LOAD 2
STORE 2
ADDRESS BUFFER 2 WRITE SIGNAL
W DATA BUFFER 2 WRITE SIGNAL 1
W DATA BUFFER 2 WRITE SIGNAL 2
ACKNOWLEDGE
BUS INTERFACE REQUEST
BUS INTERFACE READY
LOAD REGISTER 1
LOAD REGISTER 2
READY
LOAD REGISTER
INTERRUPT BY OPERATION UNIT
REGISTER FORCED WRITE SIGNAL
REGISTER FORCED READ SIGNAL
FORCED ACCESS REGISTER SIGNAL
FORCED ACCESS REGISTER NUMBER
1104-3
REGISTER FORCED ACCESS CIRCUIT
CPU REGISTER WRITE SIGNAL
CPU REGISTER READ SIGNAL
CPU ACCESS REGISTER SIGNAL
CPU DATA BUFFER READ SIGNAL
CPU DATA BUFFER WRITE SIGNAL
R DATA BUFFER 1 READ SIGNAL
R DATA BUFFER 2 READ SIGNAL
1104-4
BUS SWITCH CONTROL CIRCUIT
SWITCH 1 CONTROL
SWITCH 2 CONTROL
SWITCH 3 CONTROL

FIG. 11

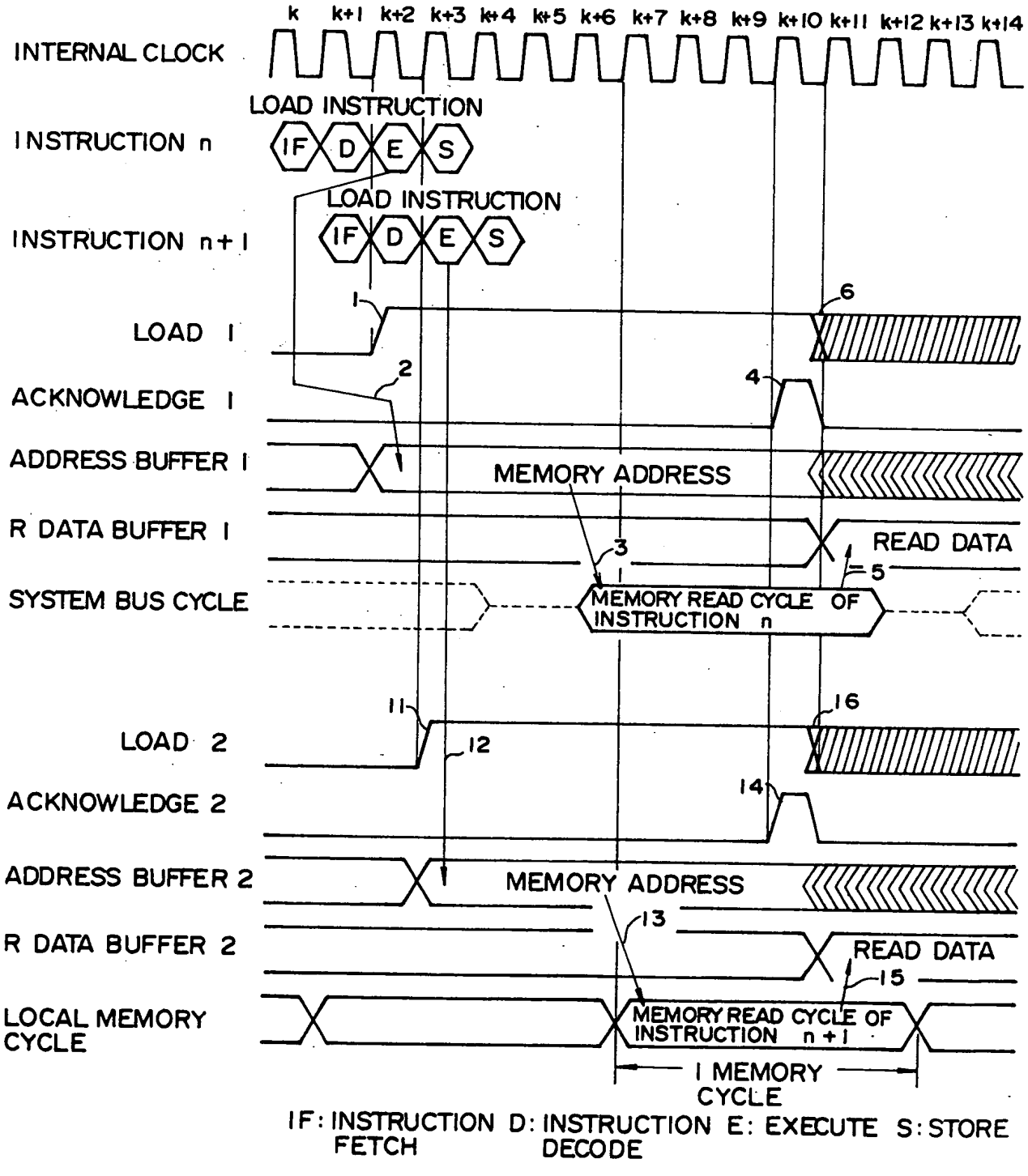
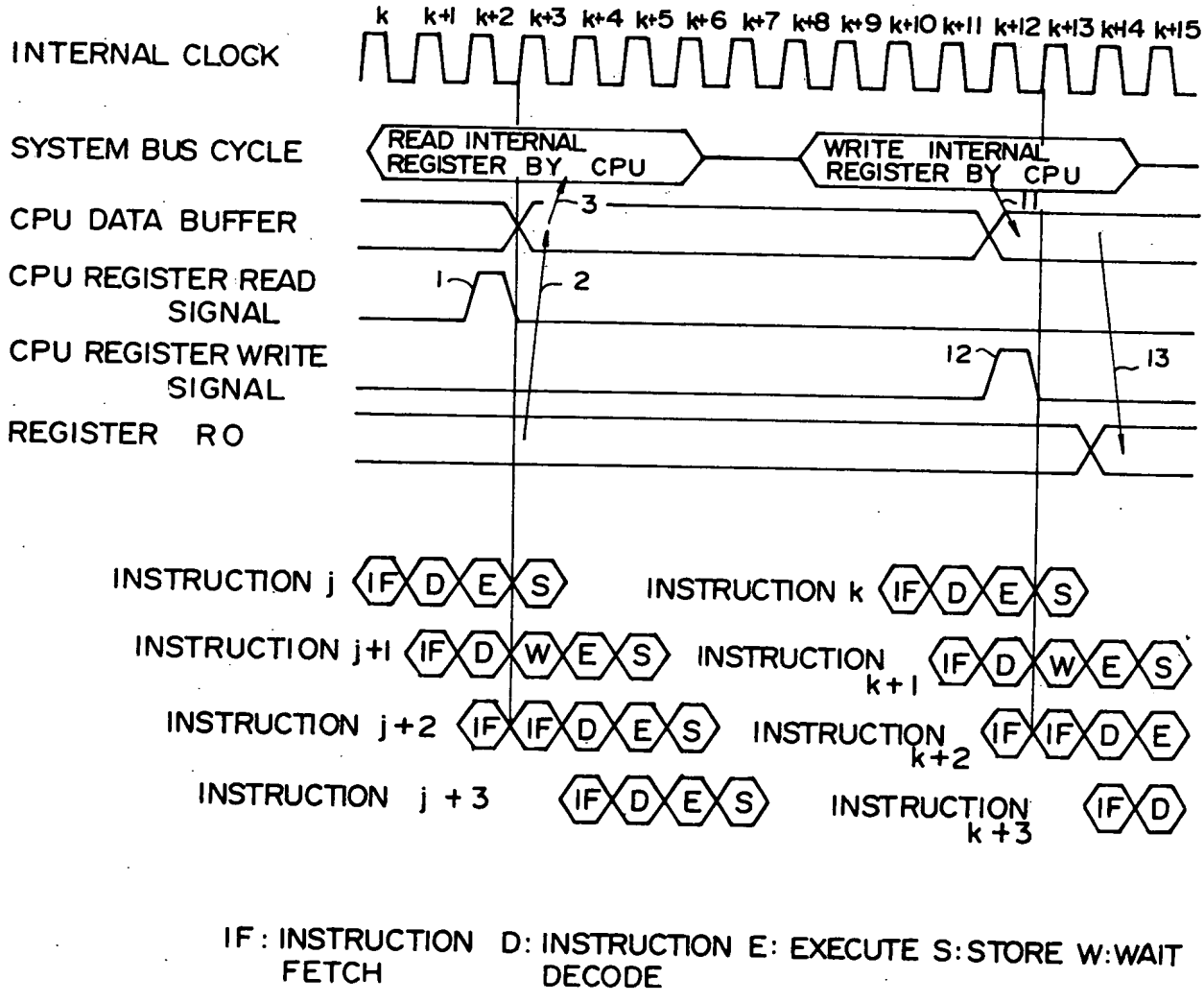

k k+1 k+2 k+3 k+4 k+5 k+6 k+7 k+8 k+9 k+10 k+11 k+12 k+13 k+14
INTERNAL CLOCK
LOAD INSTRUCTION
INSTRUCTION n
IF D E S
LOAD INSTRUCTION
INSTRUCTION n+1
IF D E S
1
6
LOAD 1
2
4
ACKNOWLEDGE 1
ADDRESS BUFFER 1
MEMORY ADDRESS
R DATA BUFFER 1
3
READ DATA
5
SYSTEM BUS CYCLE
MEMORY READ CYCLE OF INSTRUCTION n
11
16
LOAD 2
12
14
ACKNOWLEDGE 2
ADDRESS BUFFER 2
MEMORY ADDRESS
13
R DATA BUFFER 2
READ DATA
15
LOCAL MEMORY CYCLE
MEMORY READ CYCLE OF INSTRUCTION n+1
1 MEMORY CYCLE
IF: INSTRUCTION FETCH
D: INSTRUCTION DECODE
E: EXECUTE
S: STORE

FIG. 12



IF: INSTRUCTION FETCH D: INSTRUCTION DECODE E: EXECUTE S: STORE W: WAIT

FIG. 13

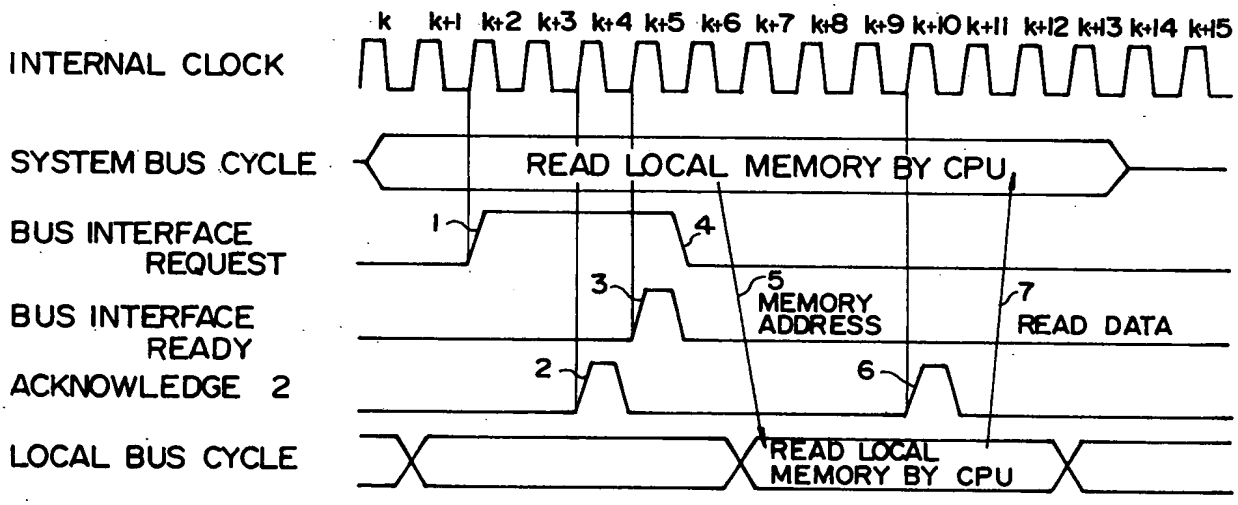

k
k+1
k+2
k+3
k+4
k+5
k+6
k+7
k+8
k+9
k+10
k+11
k+12
k+13
k+14
k+15
INTERNAL CLOCK
SYSTEM BUS CYCLE
READ LOCAL MEMORY BY CPU
BUS INTERFACE REQUEST
BUS INTERFACE READY
ACKNOWLEDGE 2
LOCAL BUS CYCLE
1
2
3
4
5
MEMORY ADDRESS
6
7
READ DATA
READ LOCAL MEMORY BY CPU

FIG. 14

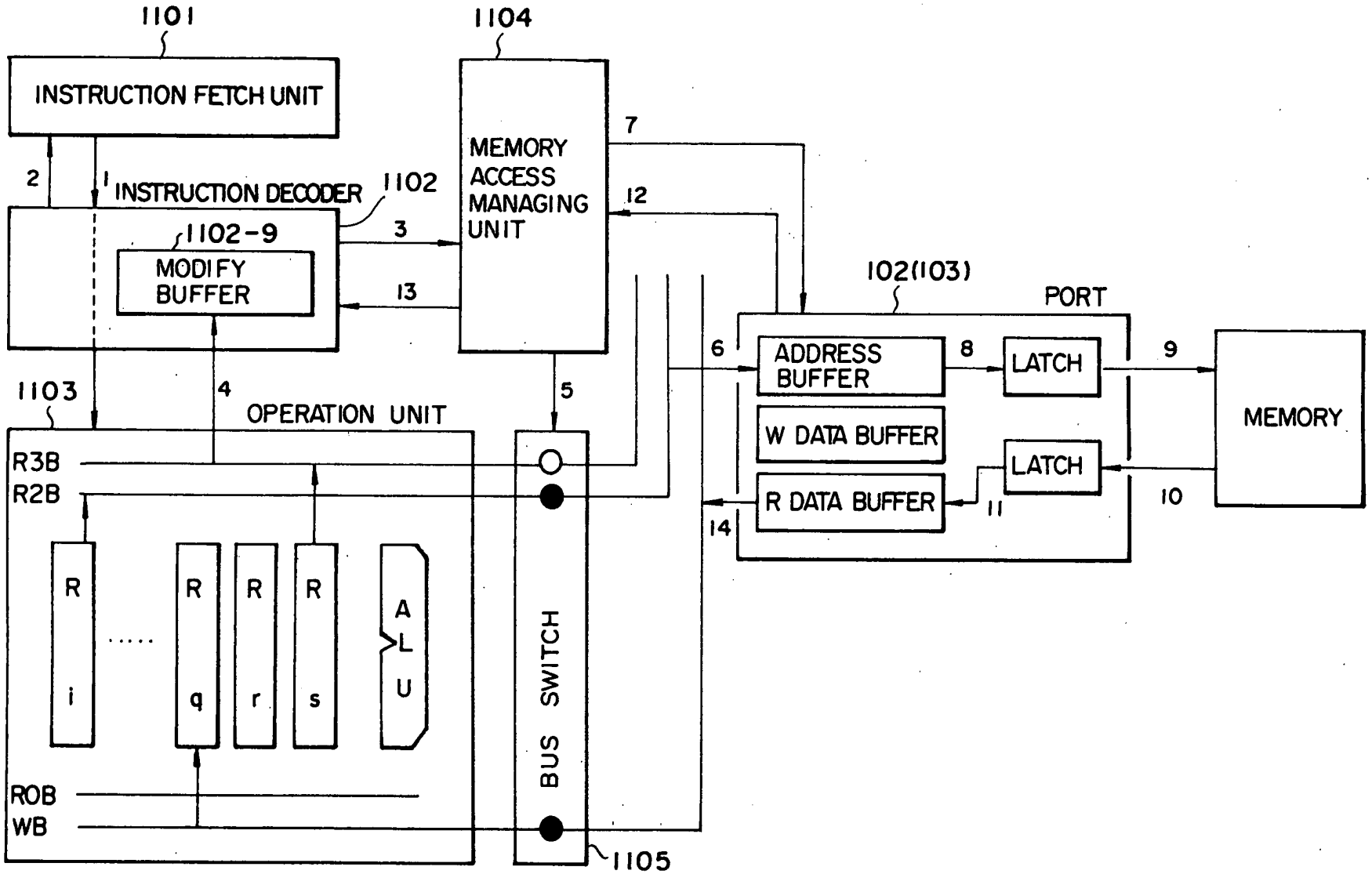

1101
INSTRUCTION FETCH UNIT
1104
MEMORY ACCESS MANAGING UNIT
2
1
INSTRUCTION DECODER
1102
1102-9
MODIFY BUFFER
3
13
7
12
102(103)
PORT
6
ADDRESS BUFFER
8
LATCH
9
MEMORY
1103
4
OPERATION UNIT
5
W DATA BUFFER
LATCH
R3B
R2B
R DATA BUFFER
11
10
14
R i
R q
R r
R s
ALU
BUS SWITCH
ROB
WB
1105

FIG. 15

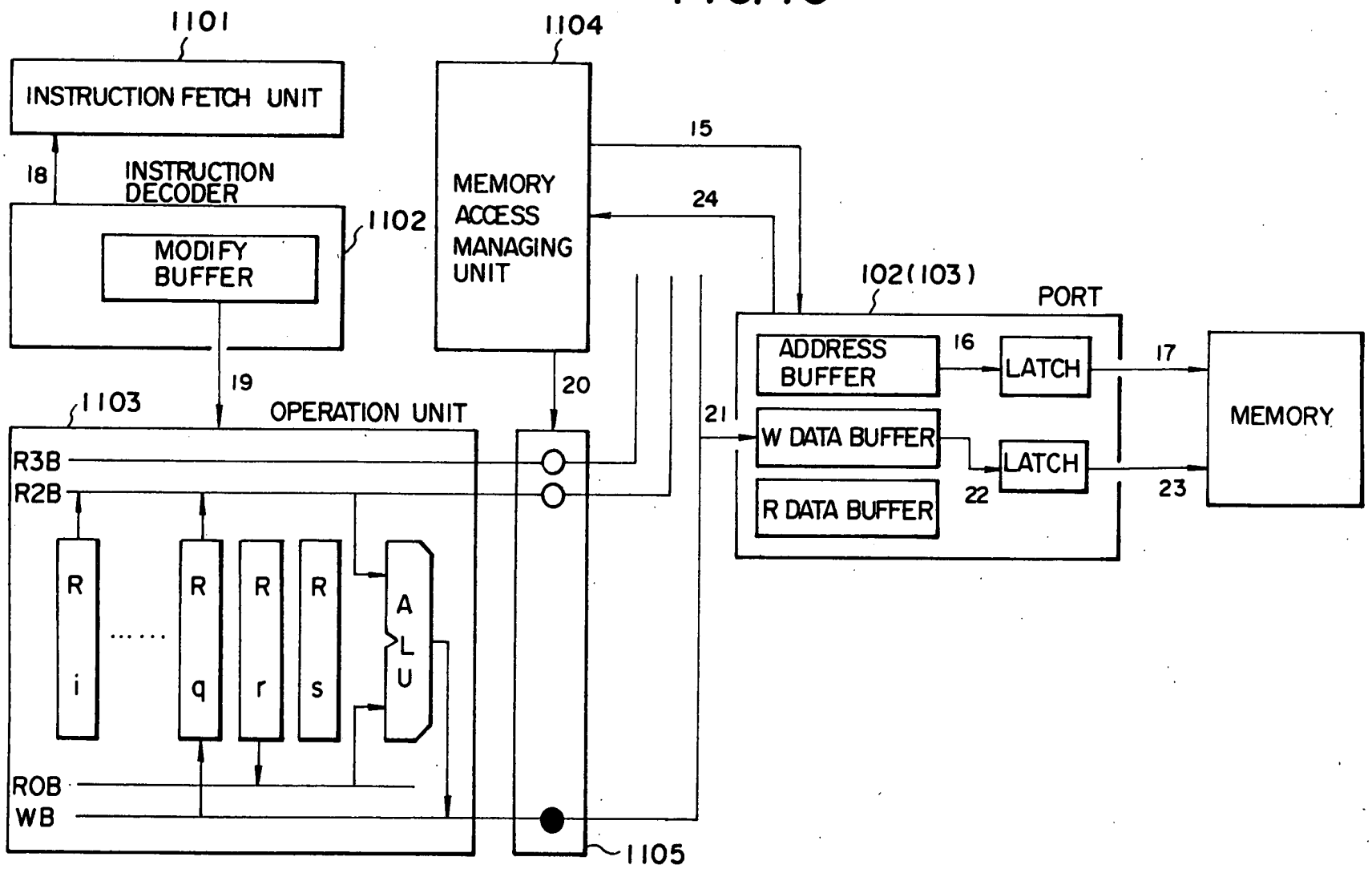
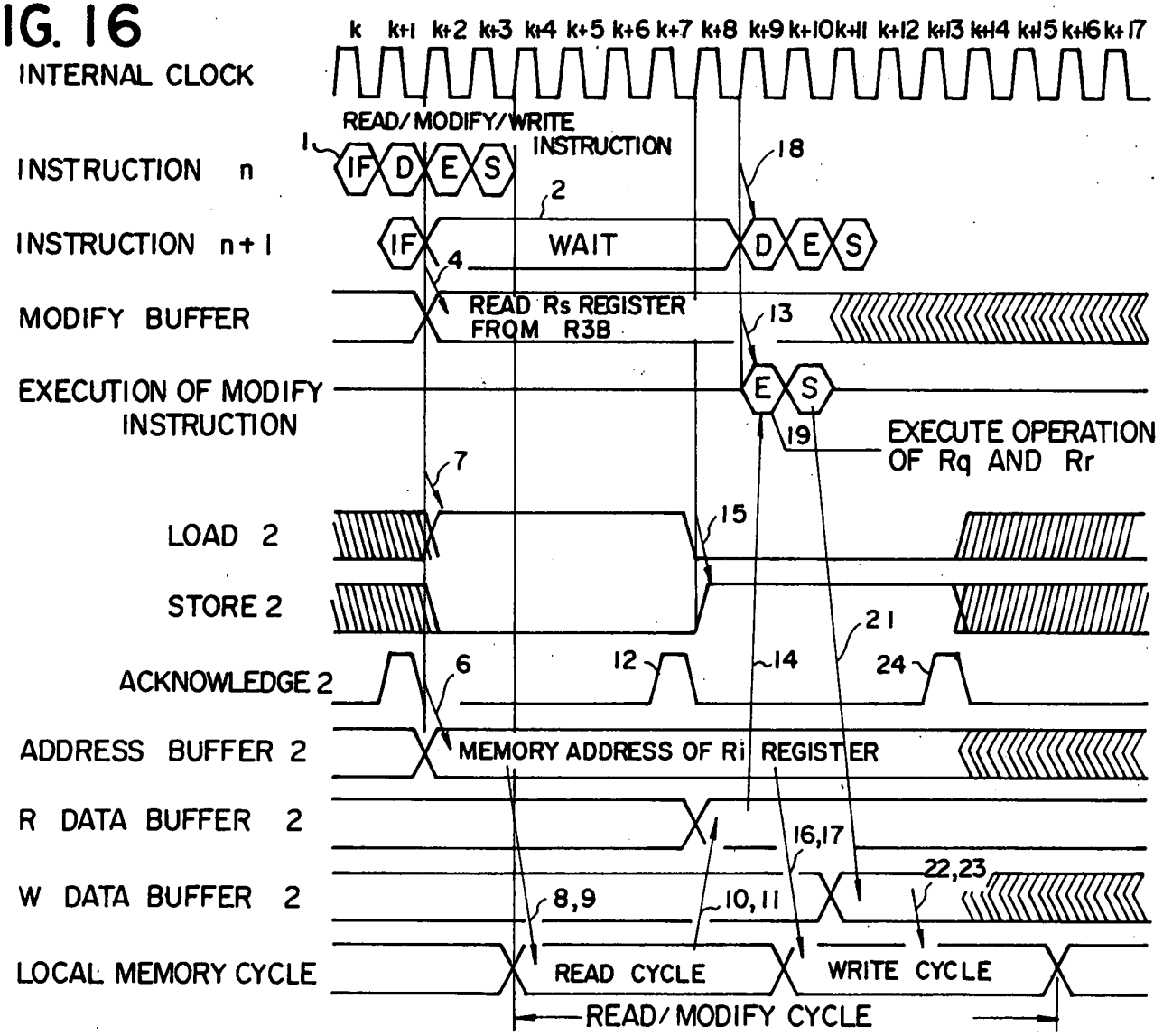

1101
INSTRUCTION FETCH UNIT
18
INSTRUCTION DECODER
1102
MODIFY BUFFER
19
1103
OPERATION UNIT
R3B
R2B
R
i
R
q
R
r
R
s
A
L
U
ROB
WB
1104
MEMORY ACCESS MANAGING UNIT
15
24
20
1105
102(103)
PORT
ADDRESS BUFFER
16
LATCH
17
21
W DATA BUFFER
LATCH
22
23
R DATA BUFFER
MEMORY

FIG. 16



IF: INSTRUCTION FETCH D: INSTRUCTION DECODE E: EXECUTE S: STORE

FIG. 17

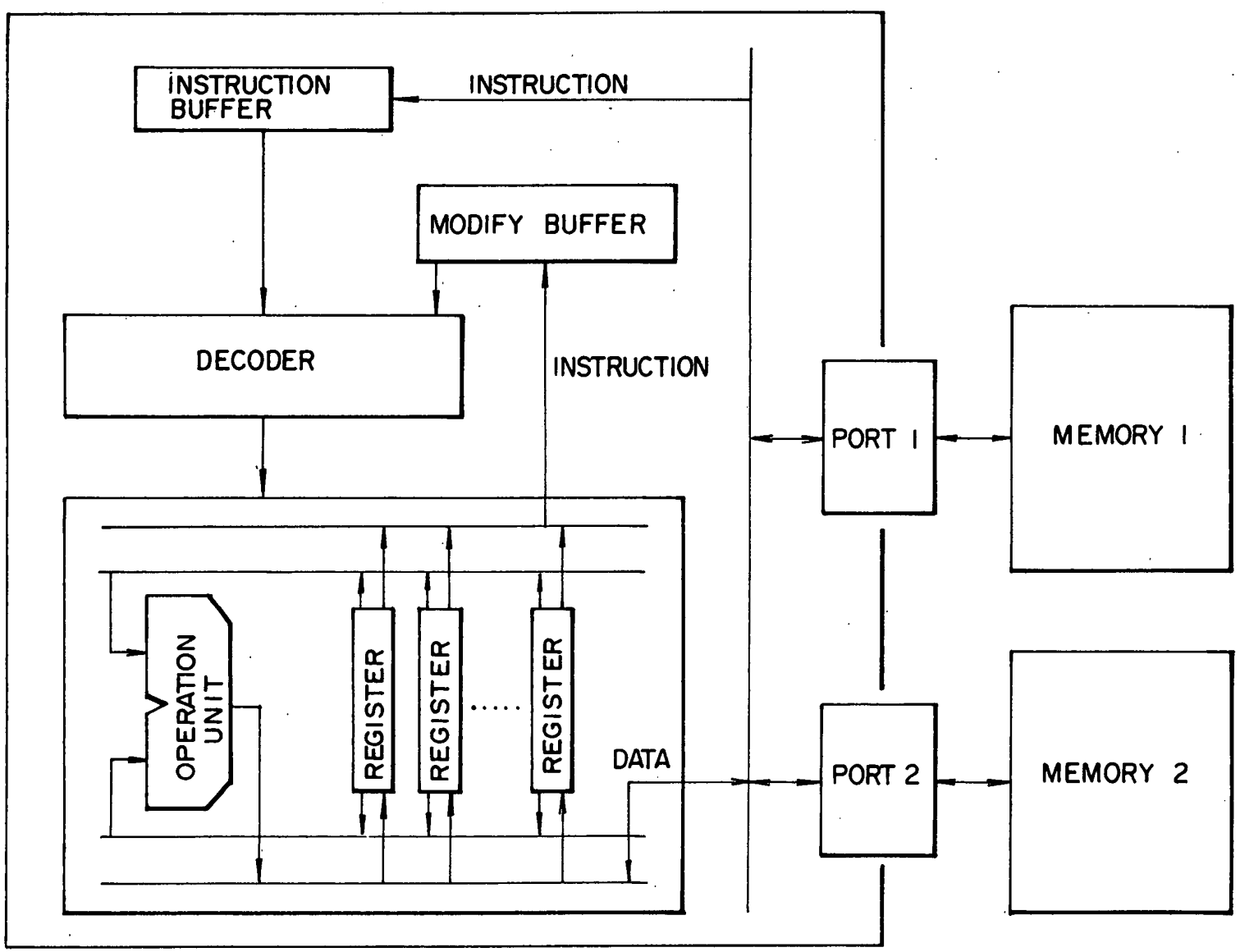

2-PORT MICROPROCESSOR
INSTRUCTION BUFFER
INSTRUCTION
MODIFY BUFFER
DECODER
INSTRUCTION
PORT 1
MEMORY 1
OPERATION UNIT
REGISTER
REGISTER
REGISTER
DATA
PORT 2
MEMORY 2

FIG. 18

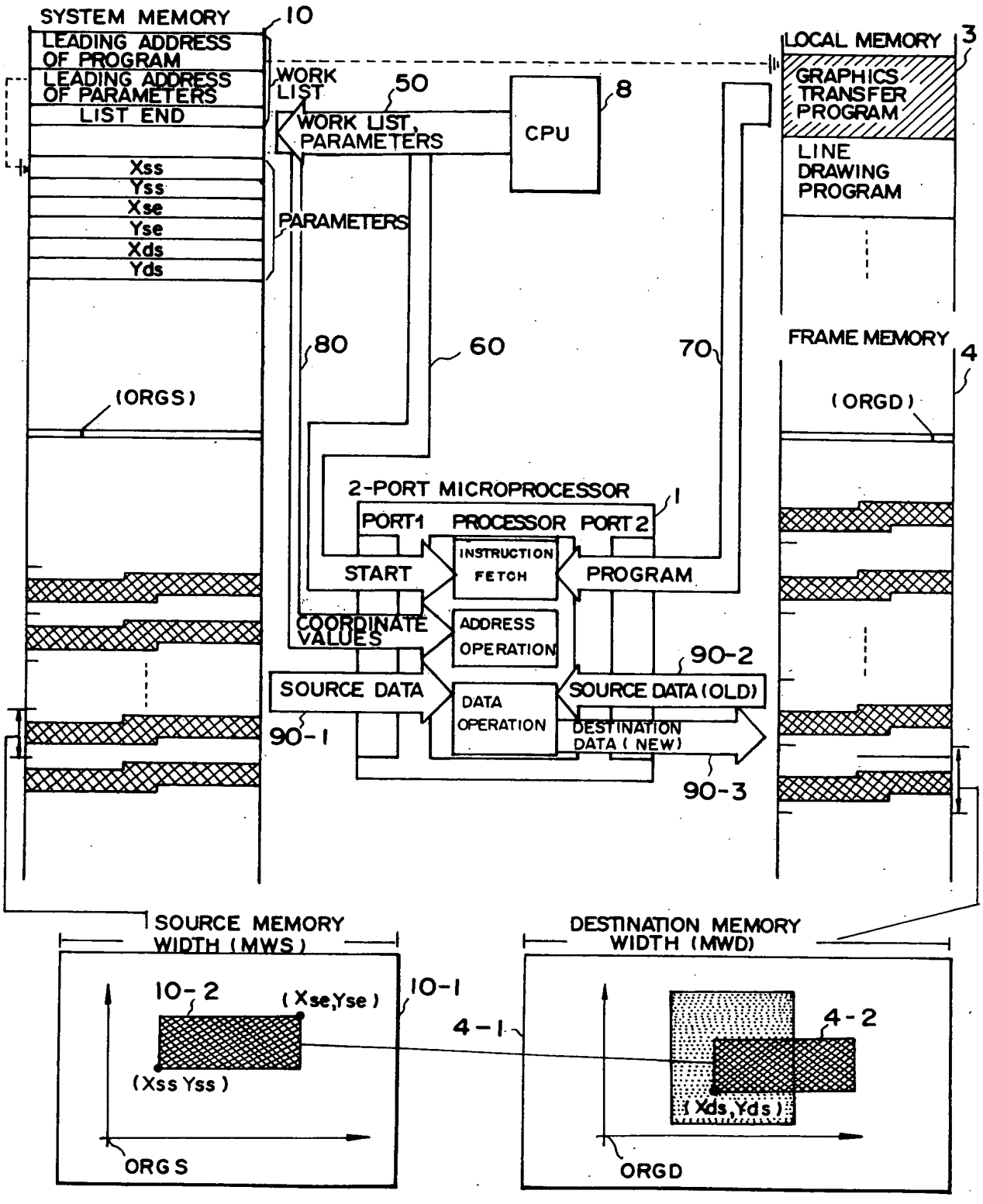
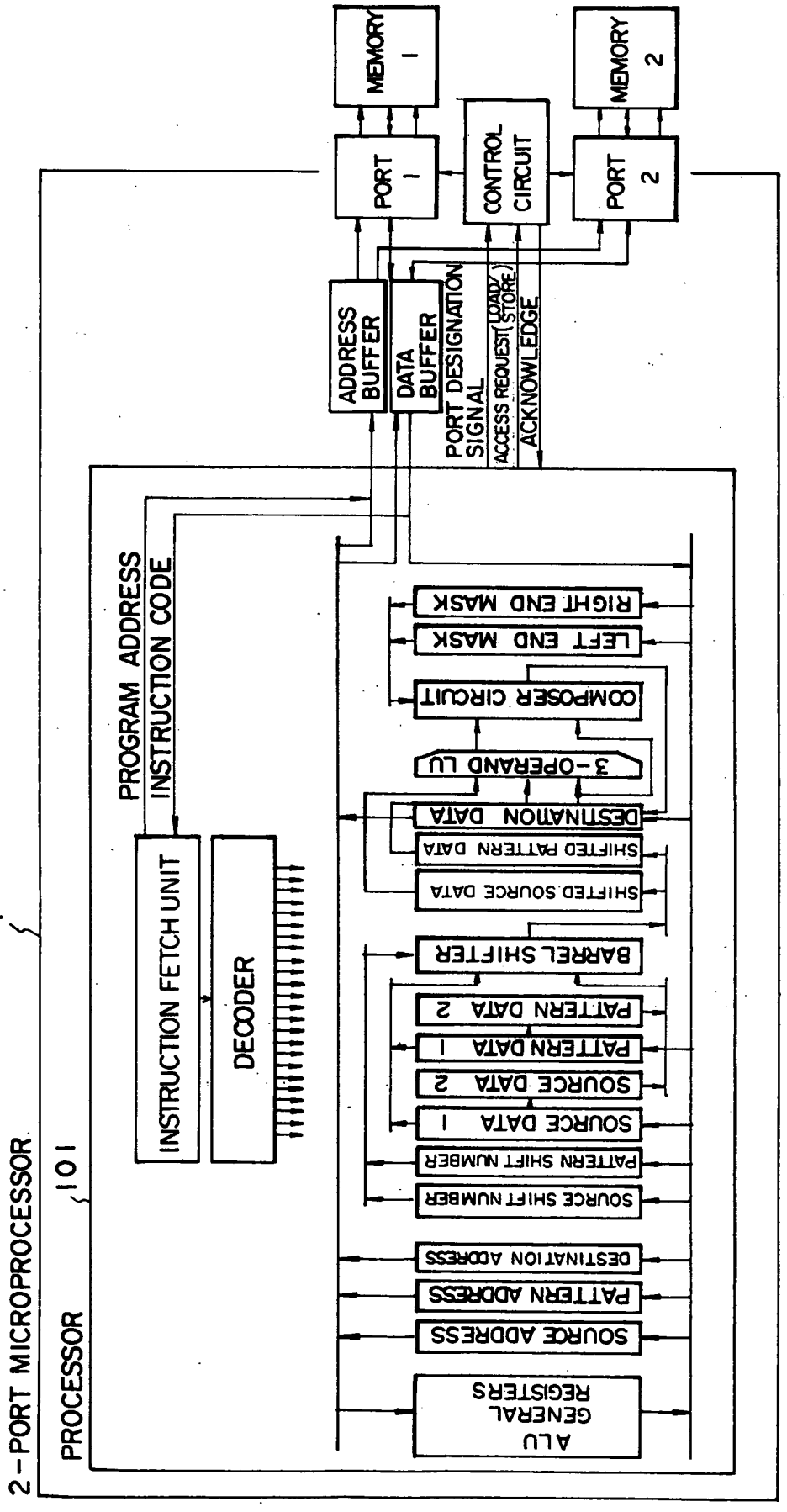

SYSTEM MEMORY
10
LEADING ADDRESS OF PROGRAM
LEADING ADDRESS OF PARAMETERS
LIST END
Xss
Yss
Xse
Yse
Xds
Yds
(ORGS)
WORK LIST
50
WORK LIST, PARAMETERS
CPU
8
PARAMETERS
80
60
70
LOCAL MEMORY
3
GRAPHICS TRANSFER PROGRAM
LINE DRAWING PROGRAM
FRAME MEMORY
4
(ORGD)
2-PORT MICROPROCESSOR
1
PORT1
PROCESSOR
PORT2
START
INSTRUCTION FETCH
PROGRAM
COORDINATE VALUES
ADDRESS OPERATION
90-2
SOURCE DATA
DATA OPERATION
SOURCE DATA (OLD)
DESTINATION DATA (NEW)
90-1
90-3
SOURCE MEMORY WIDTH (MWS)
DESTINATION MEMORY WIDTH (MWD)
10-2
(Xse,Yse)
10-1
4-1
4-2
(Xss Yss)
(Xds,Yds)
ORGS
ORGD

FIG. 19


2-PORT MICROPROCESSOR
1
PROCESSOR
101
INSTRUCTION FETCH UNIT
DECODER
PROGRAM ADDRESS
INSTRUCTION CODE
ALU
GENERAL REGISTERS
SOURCE ADDRESS
PATTERN ADDRESS
DESTINATION ADDRESS
SOURCE SHIFT NUMBER
PATTERN SHIFT NUMBER
SOURCE DATA 1
SOURCE DATA 2
PATTERN DATA 1
PATTERN DATA 2
BARREL SHIFTER
SHIFTED SOURCE DATA
SHIFTED PATTERN DATA
DESTINATION DATA
3-OPERAND LU
COMPOSER CIRCUIT
LEFT END MASK
RIGHT END MASK
ADDRESS BUFFER
DATA BUFFER
PORT DESIGNATION SIGNAL
ACCESS REQUEST (LOAD/STORE)
ACKNOWLEDGE
PORT 1
CONTROL CIRCUIT
PORT 2
MEMORY 1
MEMORY 2